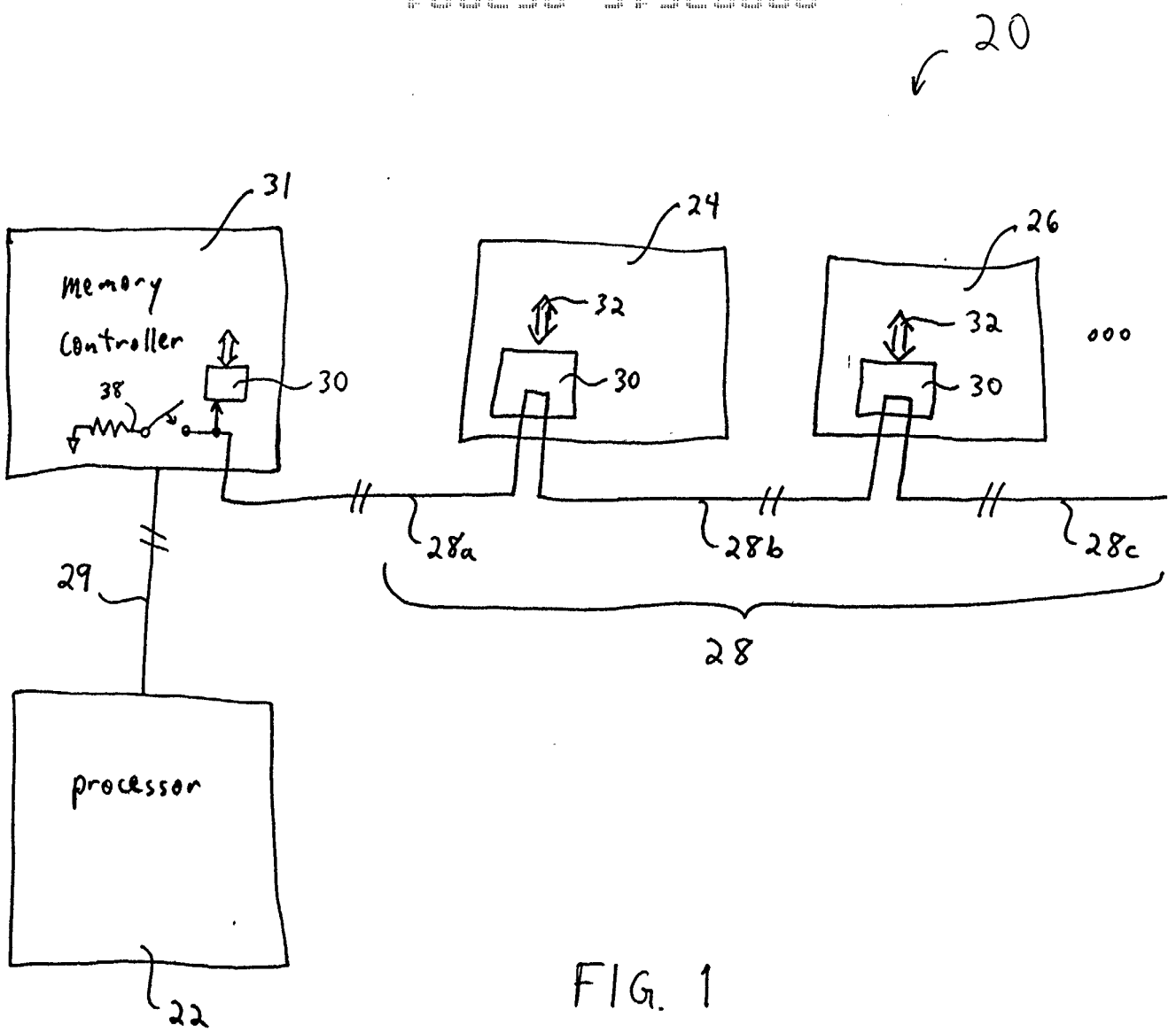


FIG. 1

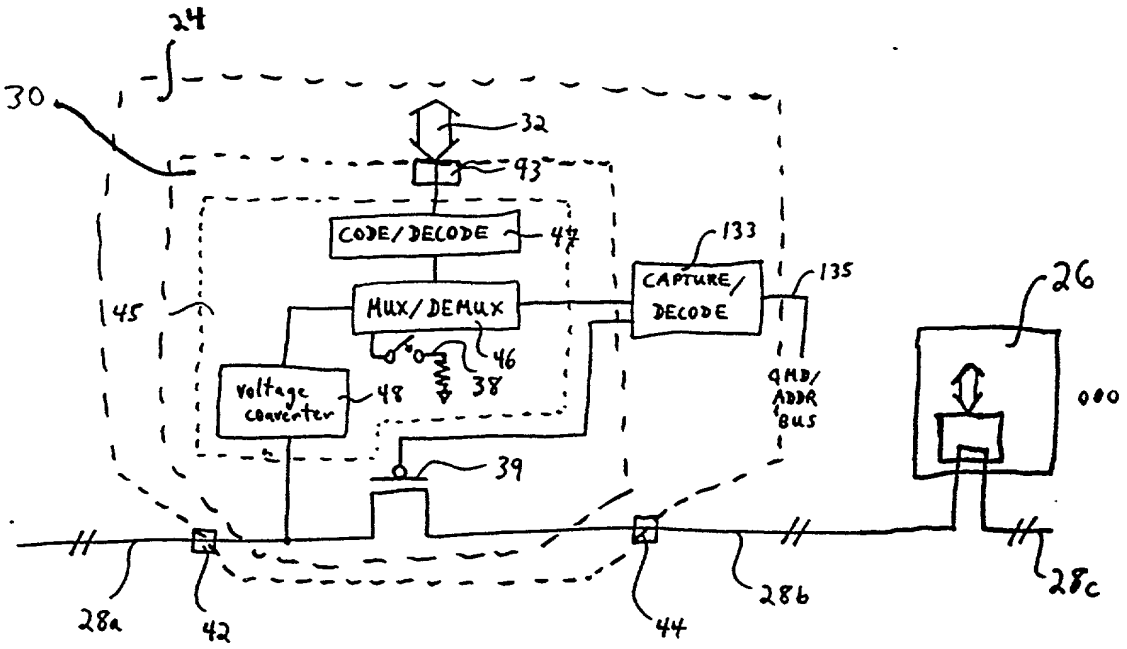

24
30
32
43
CODE/DECODE
47
133
CAPTURE/
DECODE
135
26
45
MUX/DEMUX
46
Voltage
converter
48
38
CMD/
ADDR
BUS
000
39
28a
42
44
28b
28c

FIG. 2

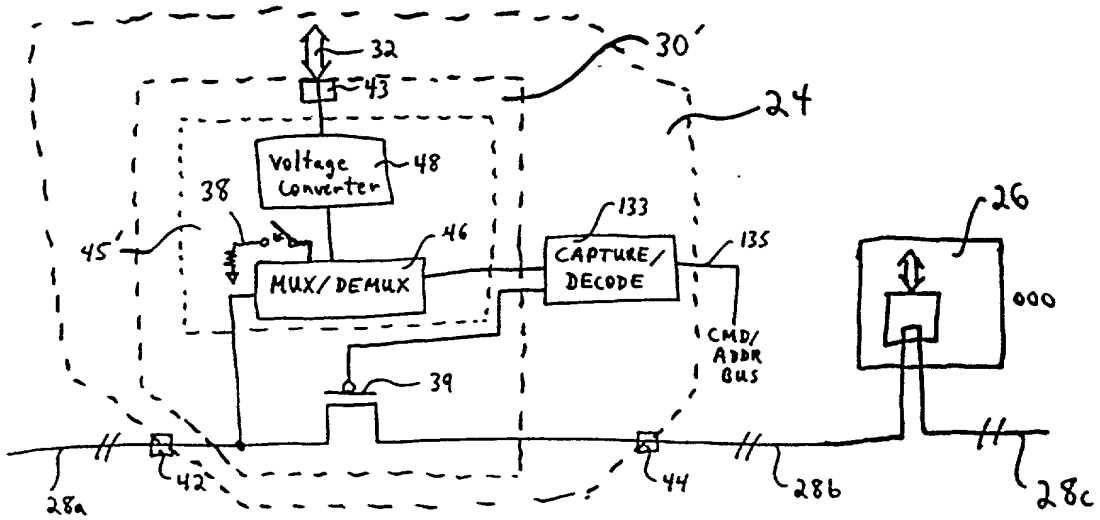

32
30'
43
24
Voltage
Converter
48
38
133
26
45'
46
CAPTURE/
DECODE
135
MUX/DEMUX
000
CMD/
ADDR
BUS
39
42
44
28b
28a
28c

FIG. 3

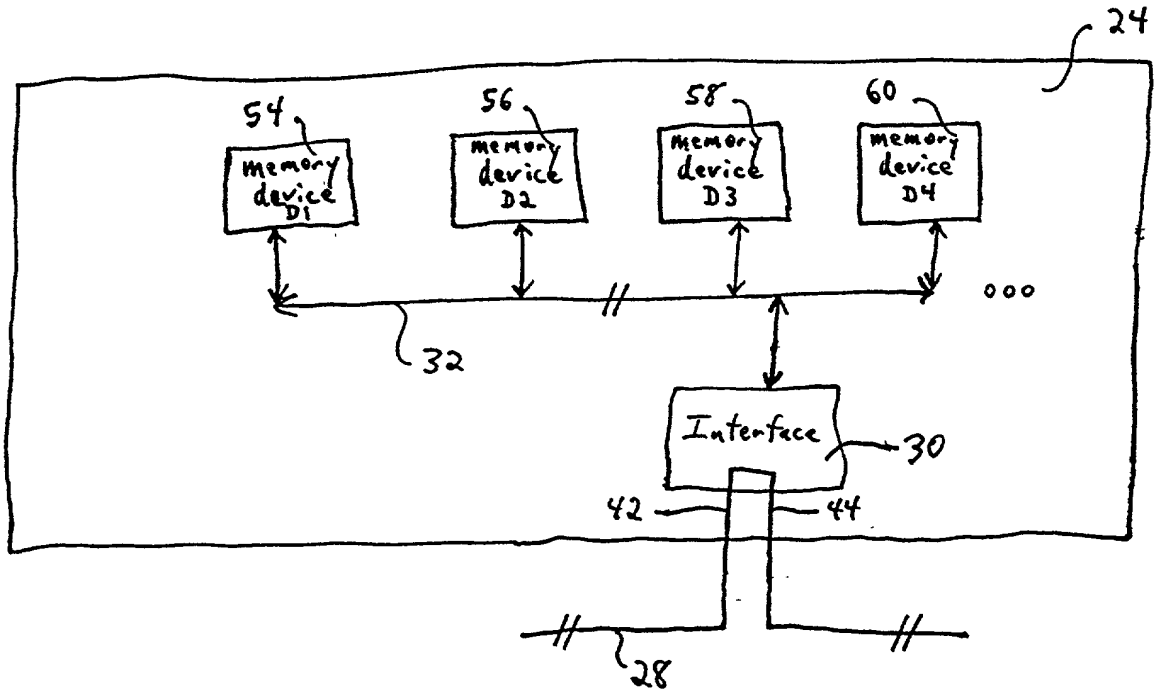

24
54
memory device D1
56
memory device D2
58
memory device D3
60
memory device D4
000
32
Interface
30
42
44
28

FIG. 4

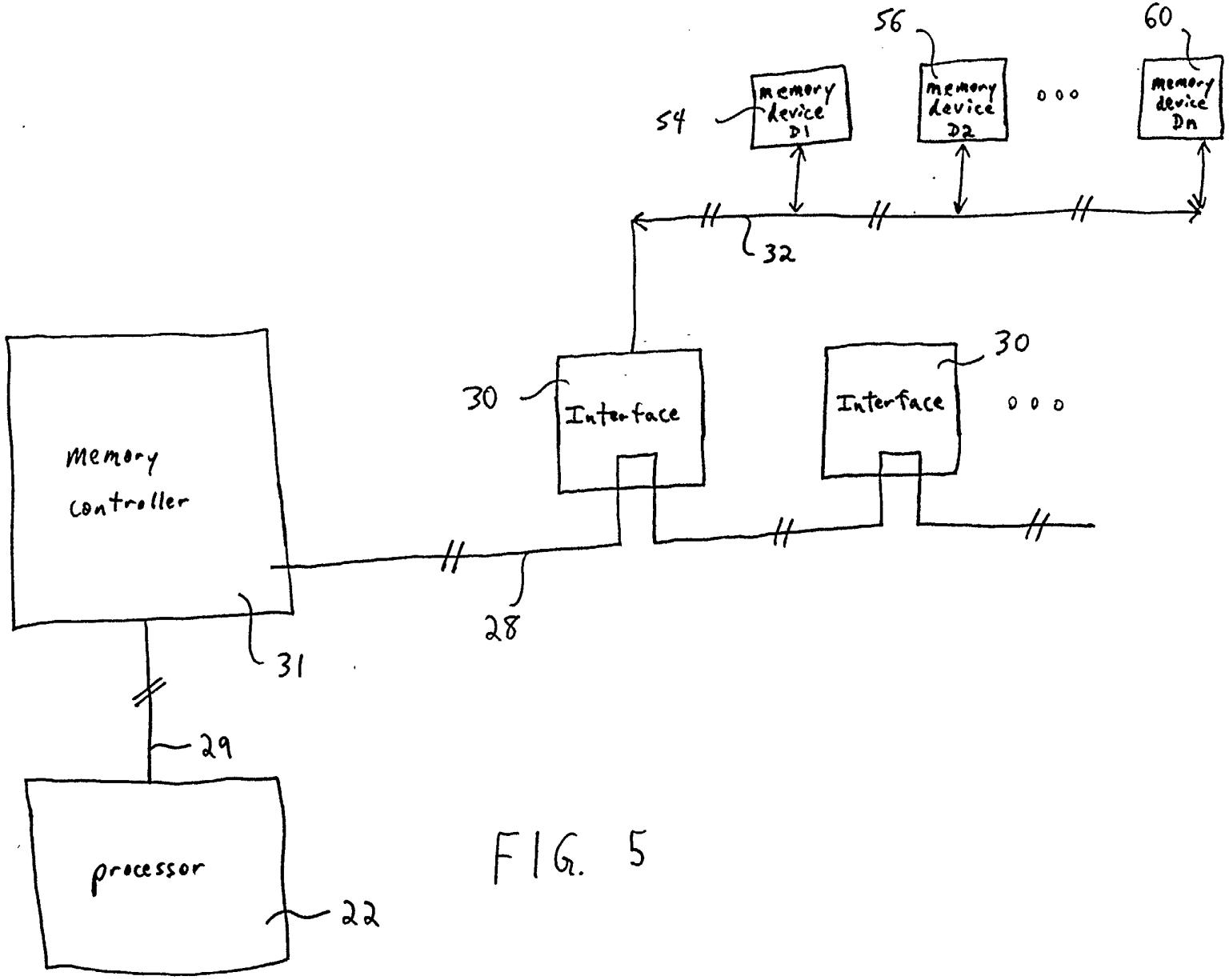

56
60
54
memory device D1
memory device D2
memory device Dn
32
30
Interface
30
Interface
memory controller
28
31
29
processor
22

FIG. 5

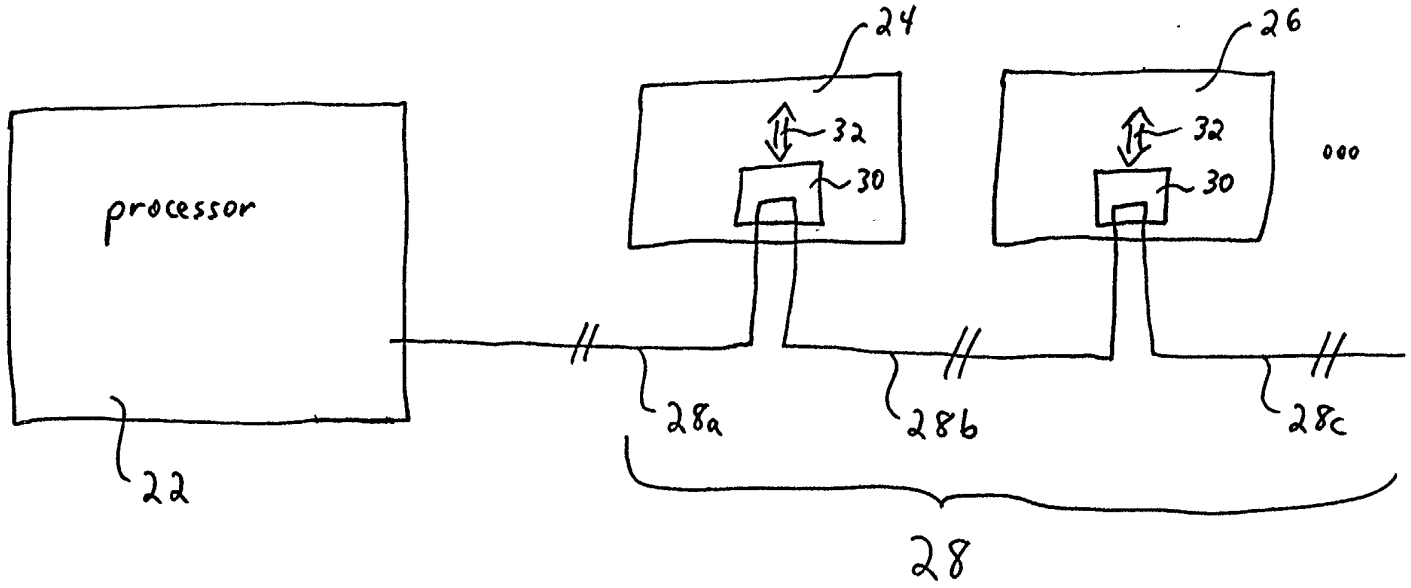


FIG. 6

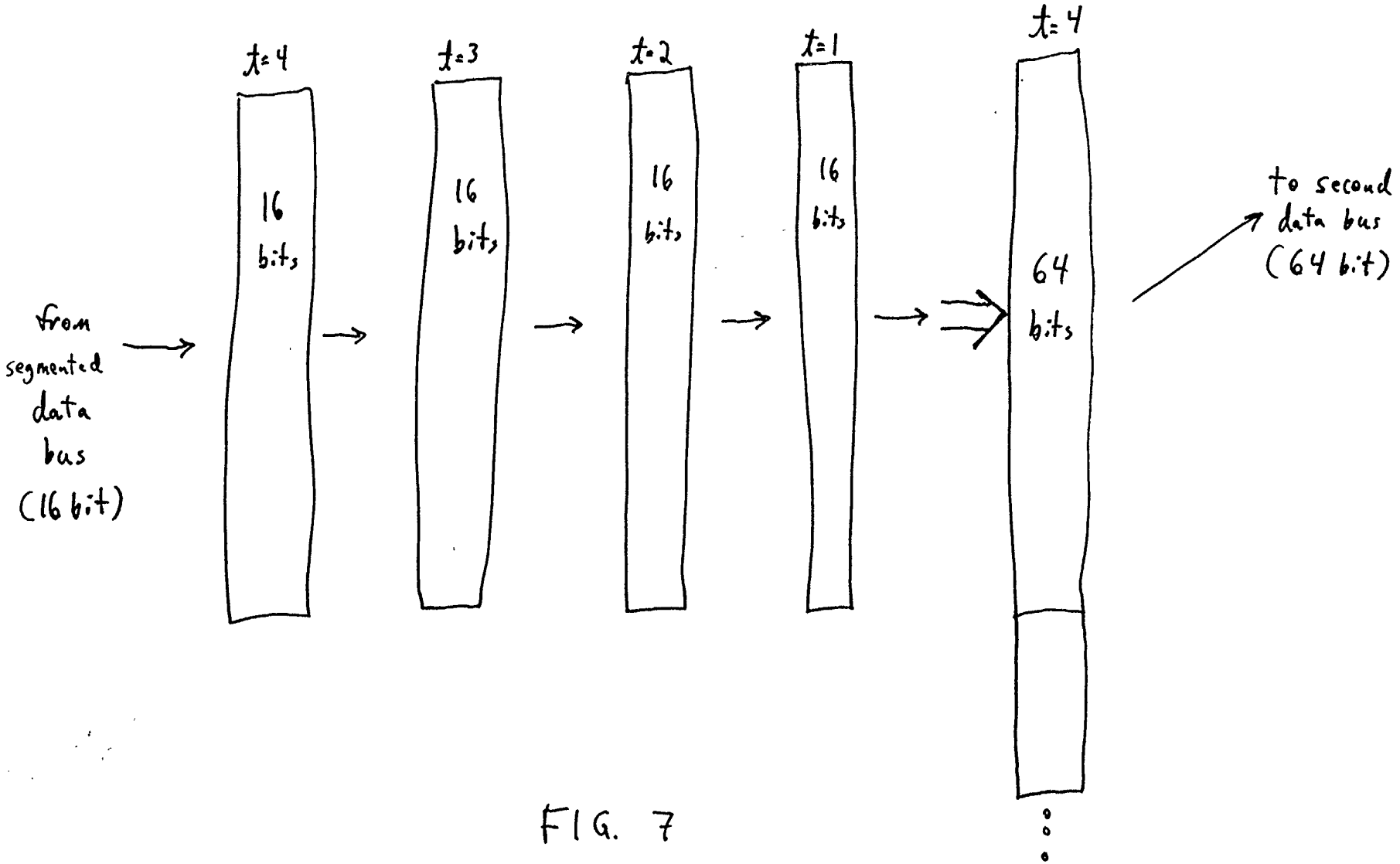


FIG. 7

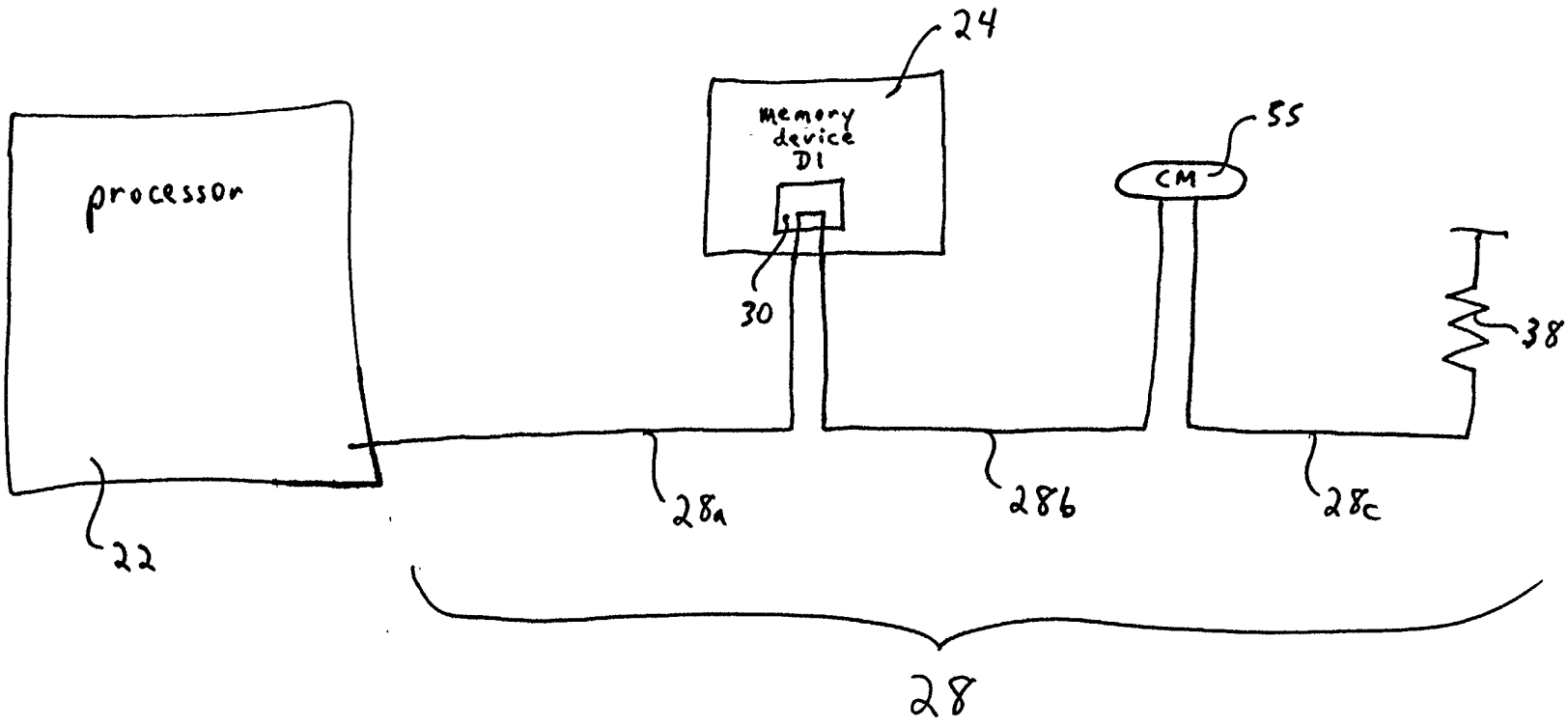
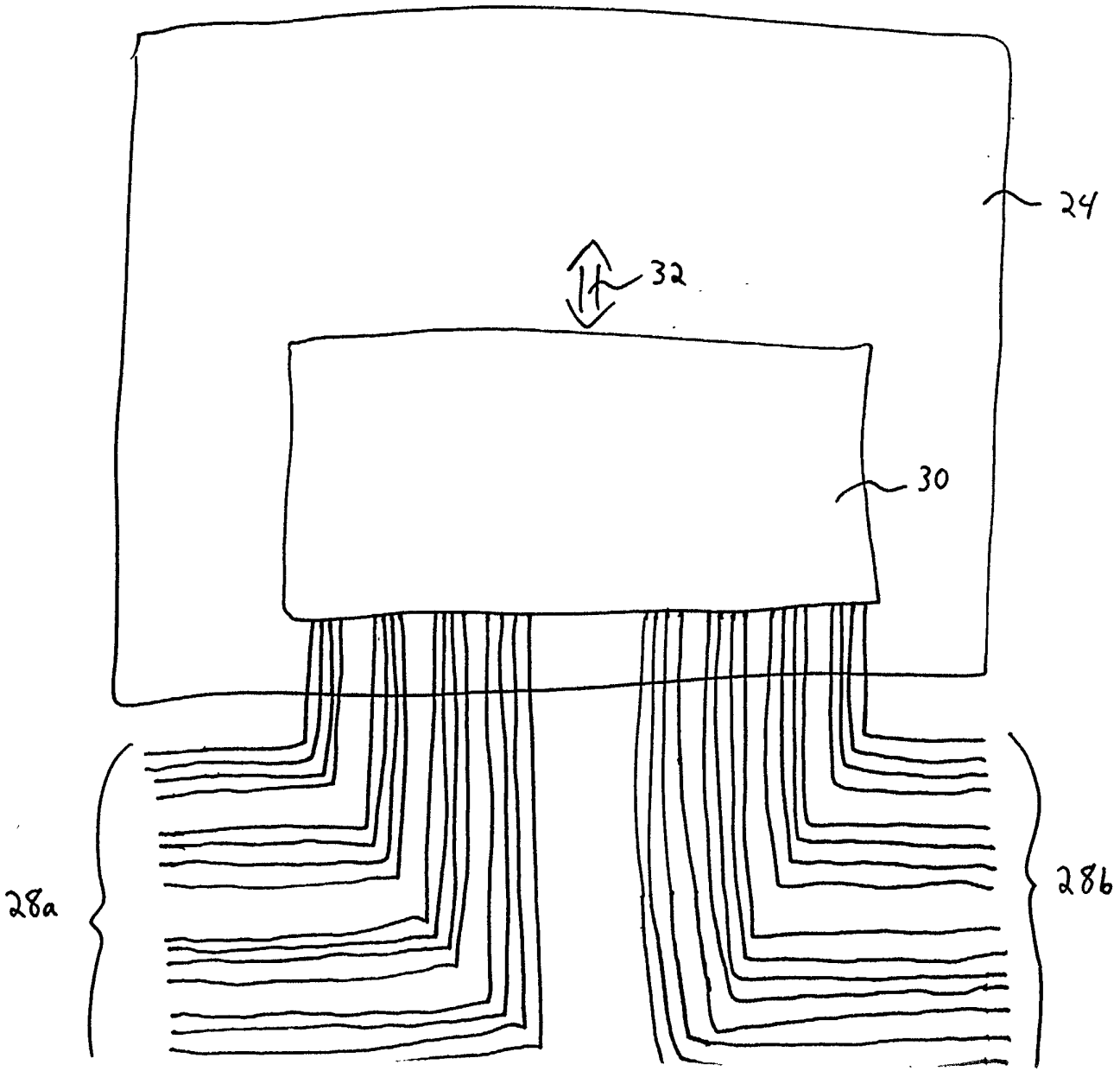


FIG. 8

FIG. 9



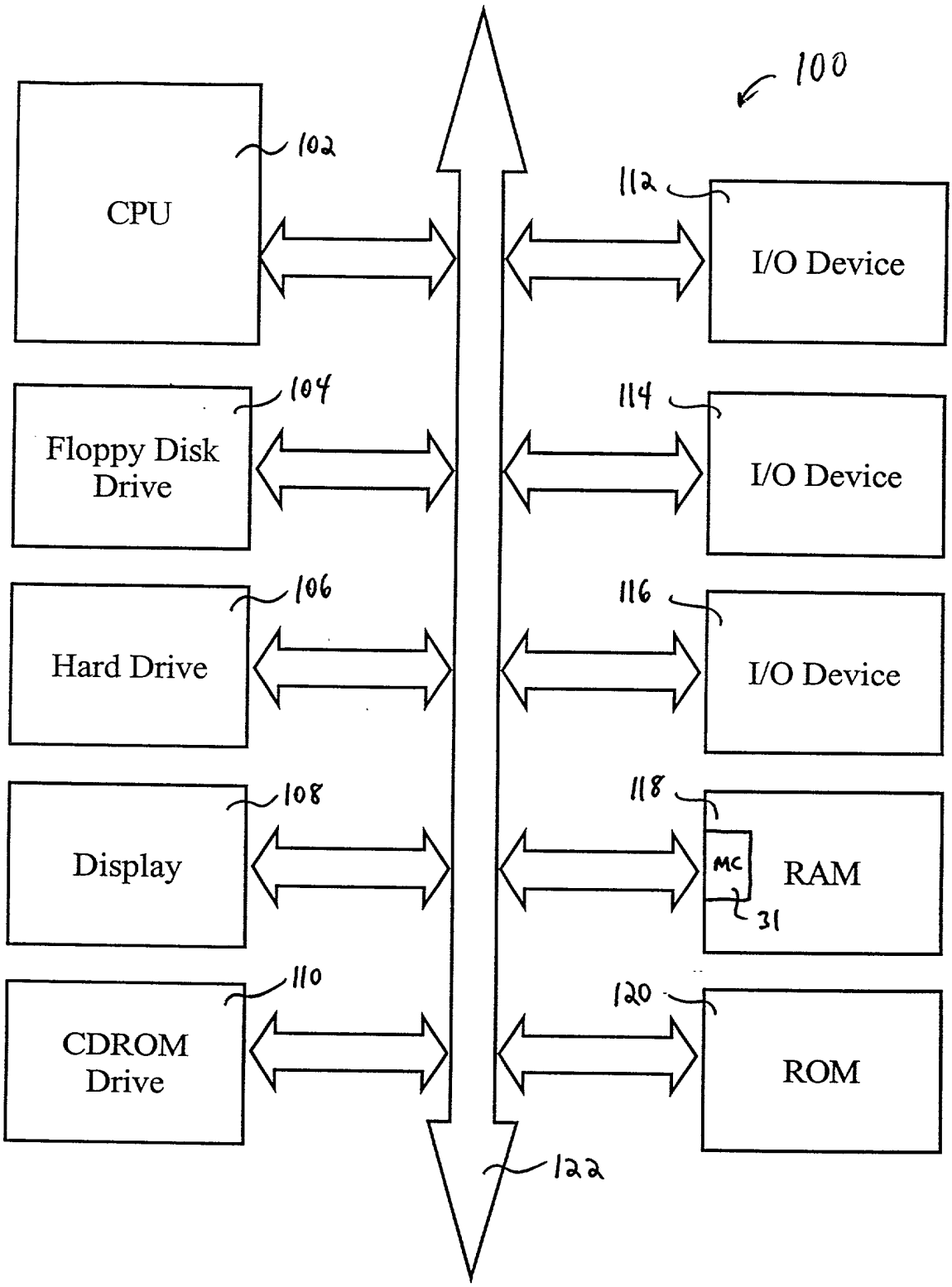

100
CPU
102
Floppy Disk Drive
104
Hard Drive
106
Display
108
CDROM Drive
110
112
I/O Device
114
I/O Device
116
I/O Device
118
MC
RAM
31
120
ROM
122

FIG. 10

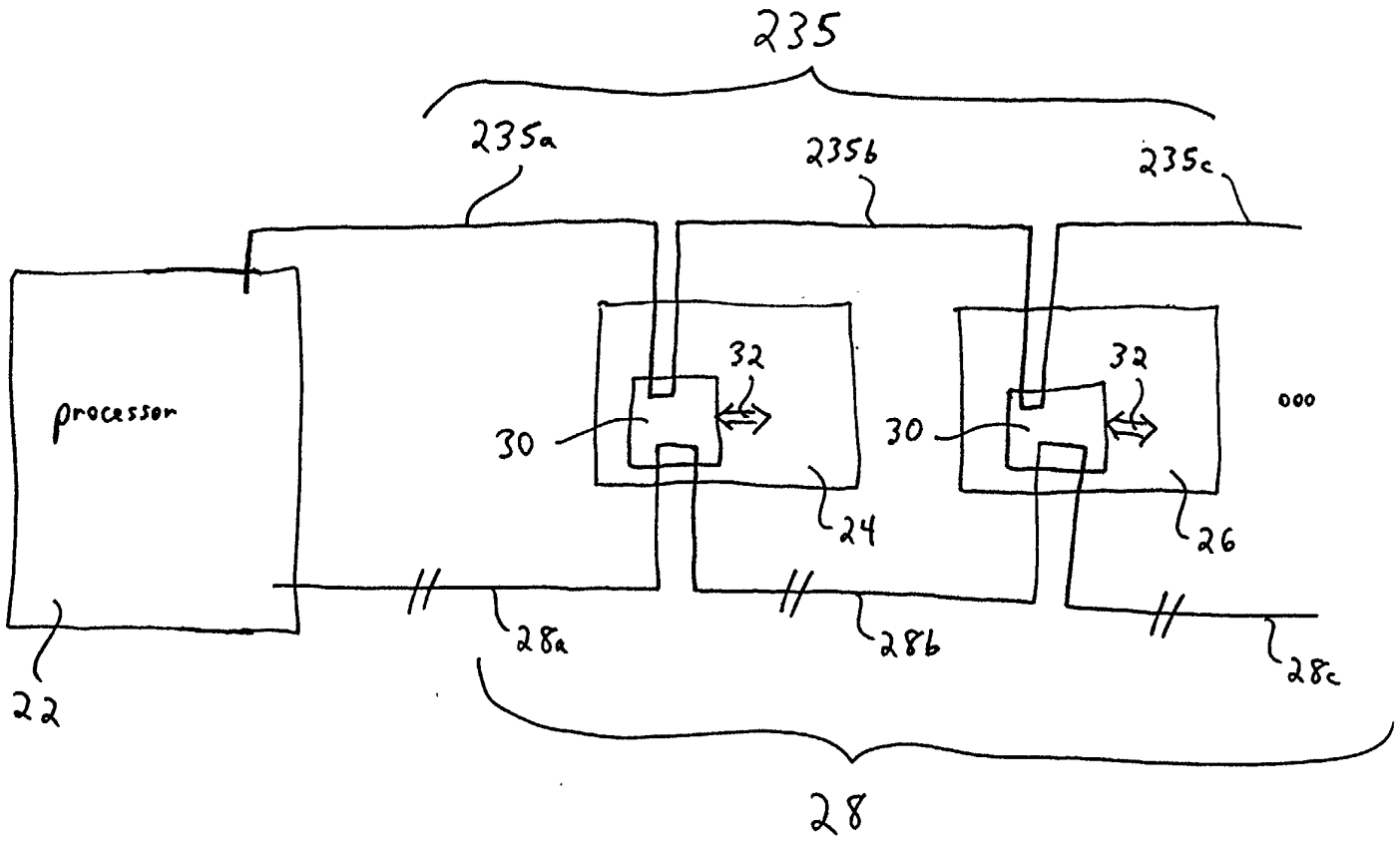


FIG. 11

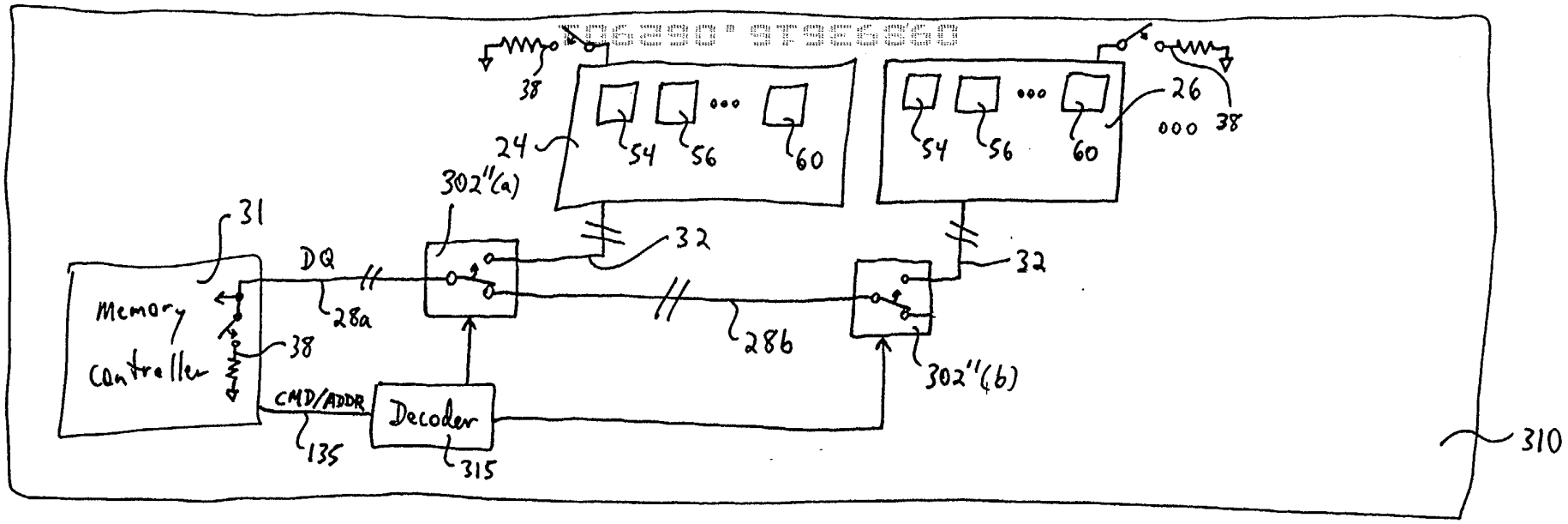

38
24
54
56
60
26
38
302"(a)
31
32
32
DQ
28a
28b
Memory
controller
38
CMD/ADDR
135
Decoder
315
302"(b)
310

FIG. 12

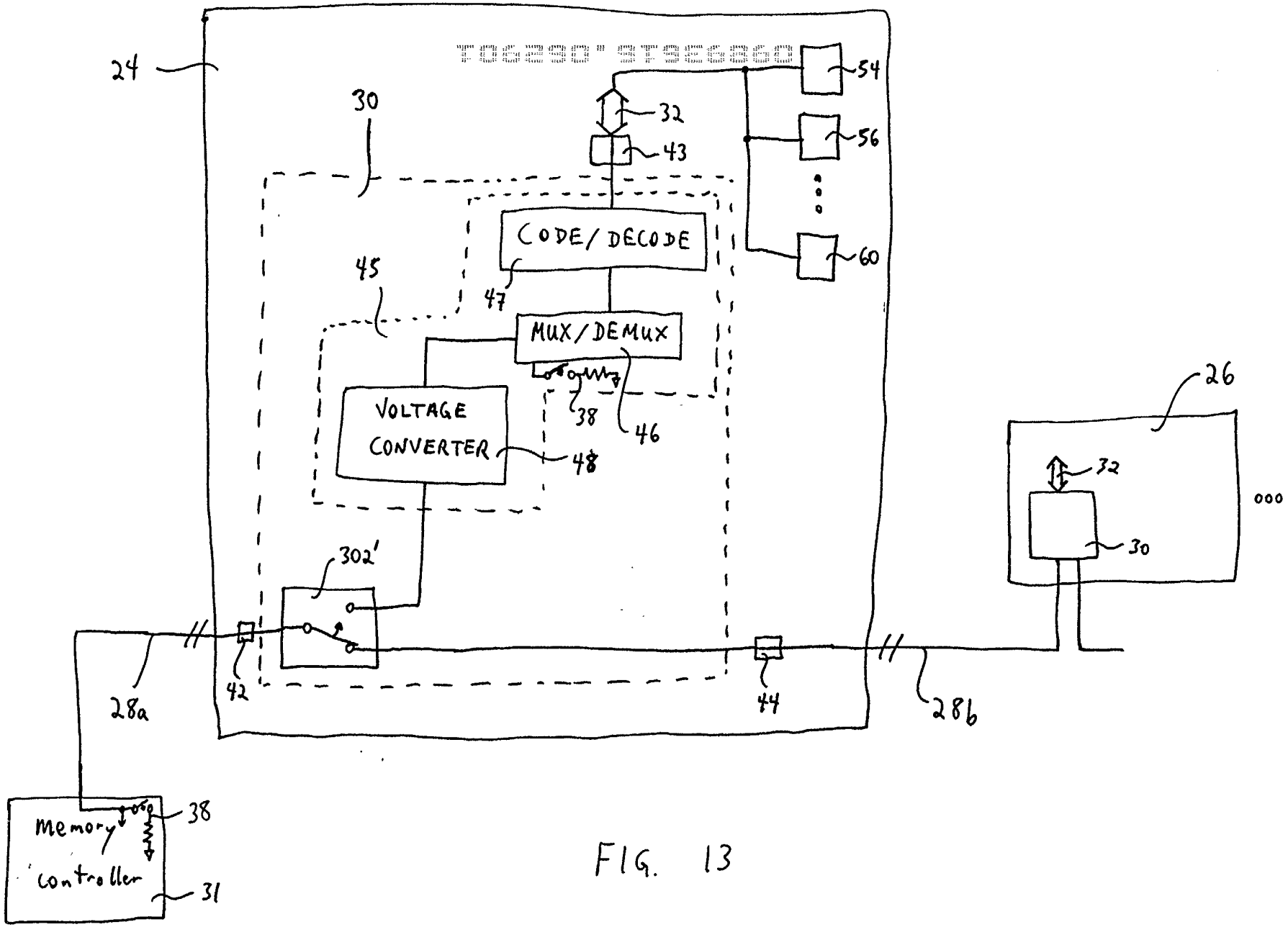

24
30
32
43
54
56
60
CODE/DECODE
47
45
MUX/DEMUX
38
46
VOLTAGE CONVERTER
48
302'
42
44
28a
28b
26
32
30
000
Memory controller
38
31

FIG. 13

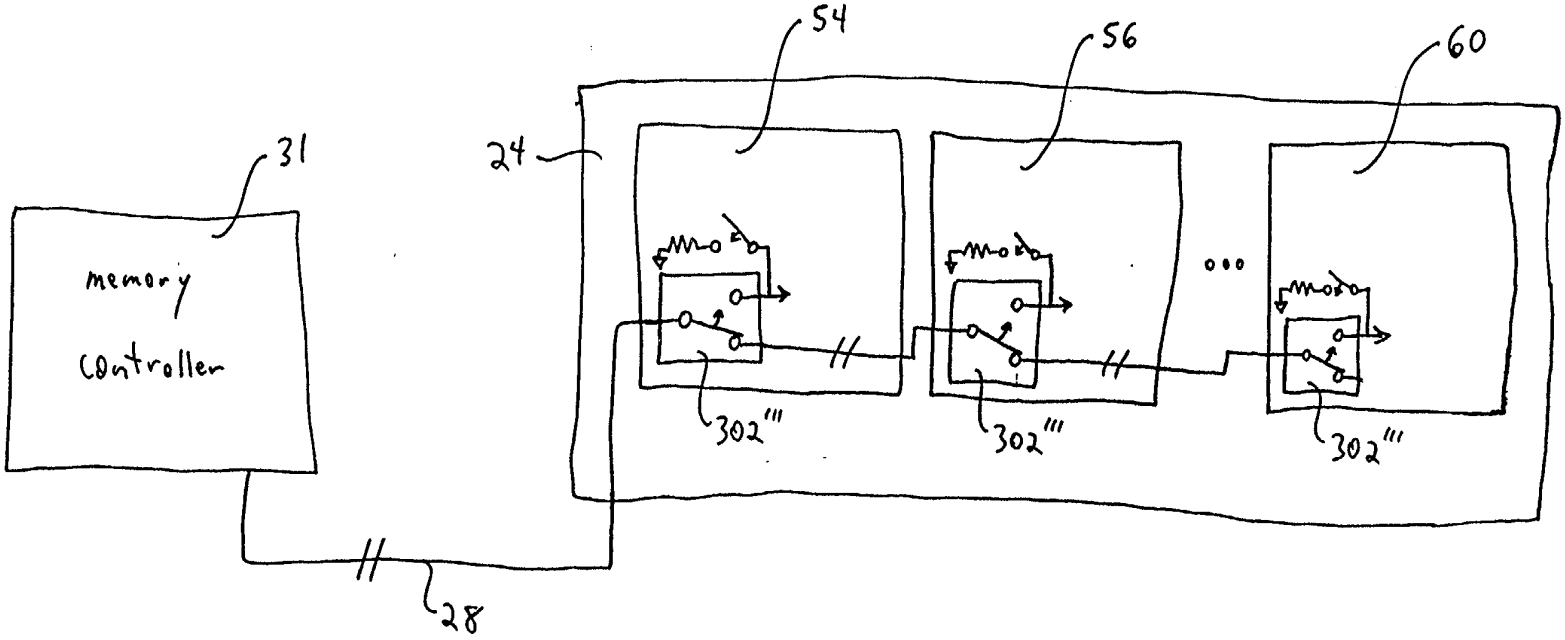


FIG. 14

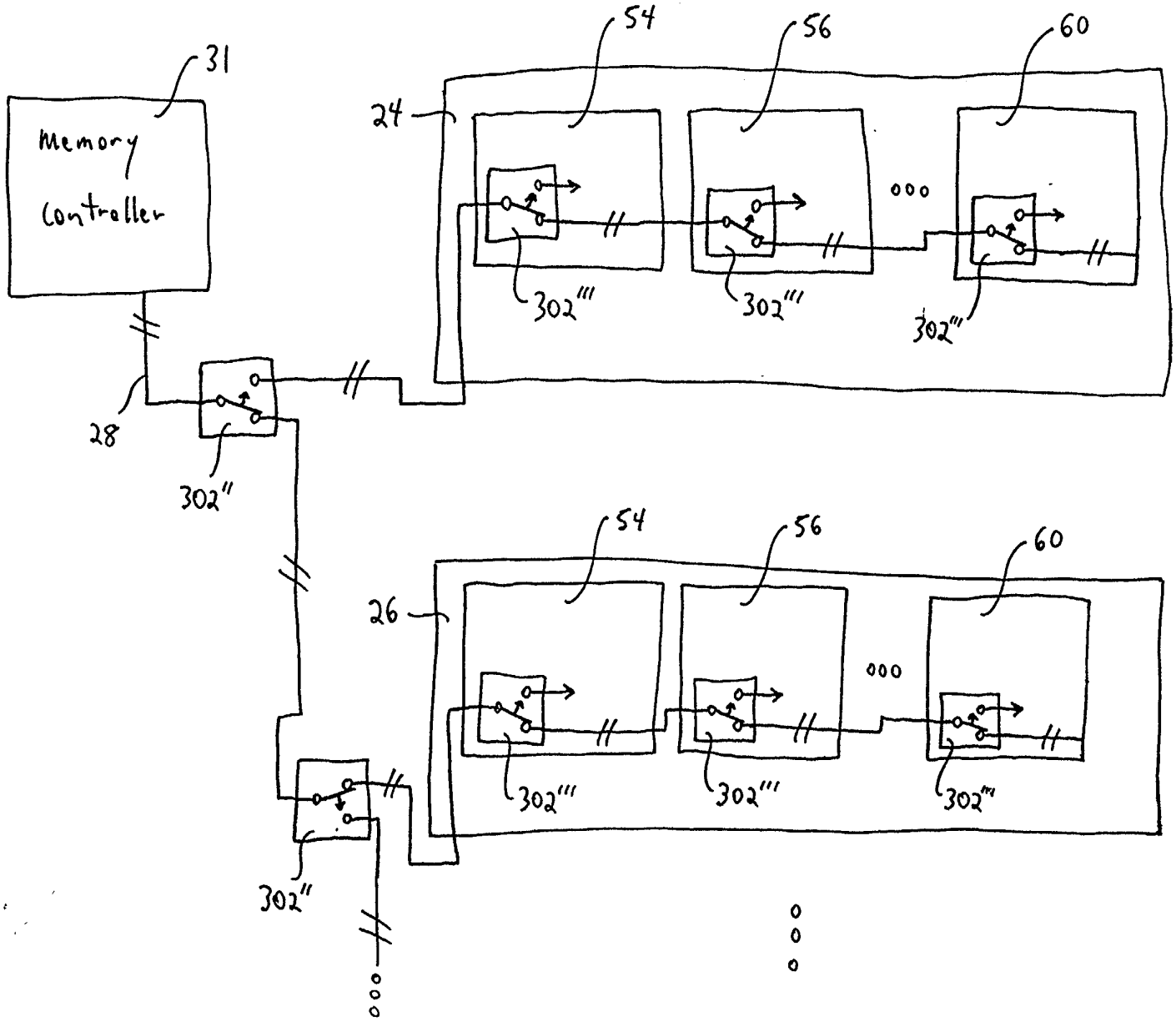

31
Memory
Controller
24
54
56
60
302'''
302'''
302'''
28
302''
26
54
56
60
302'''
302'''
302'''
302''

FIG. 15

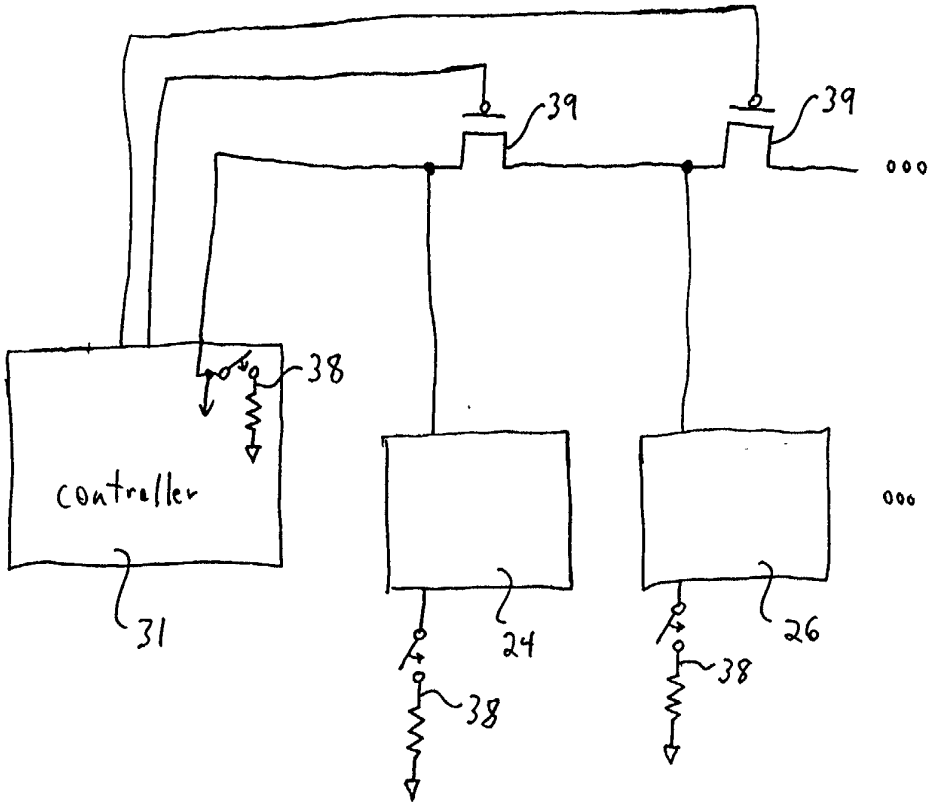


FIG. 16

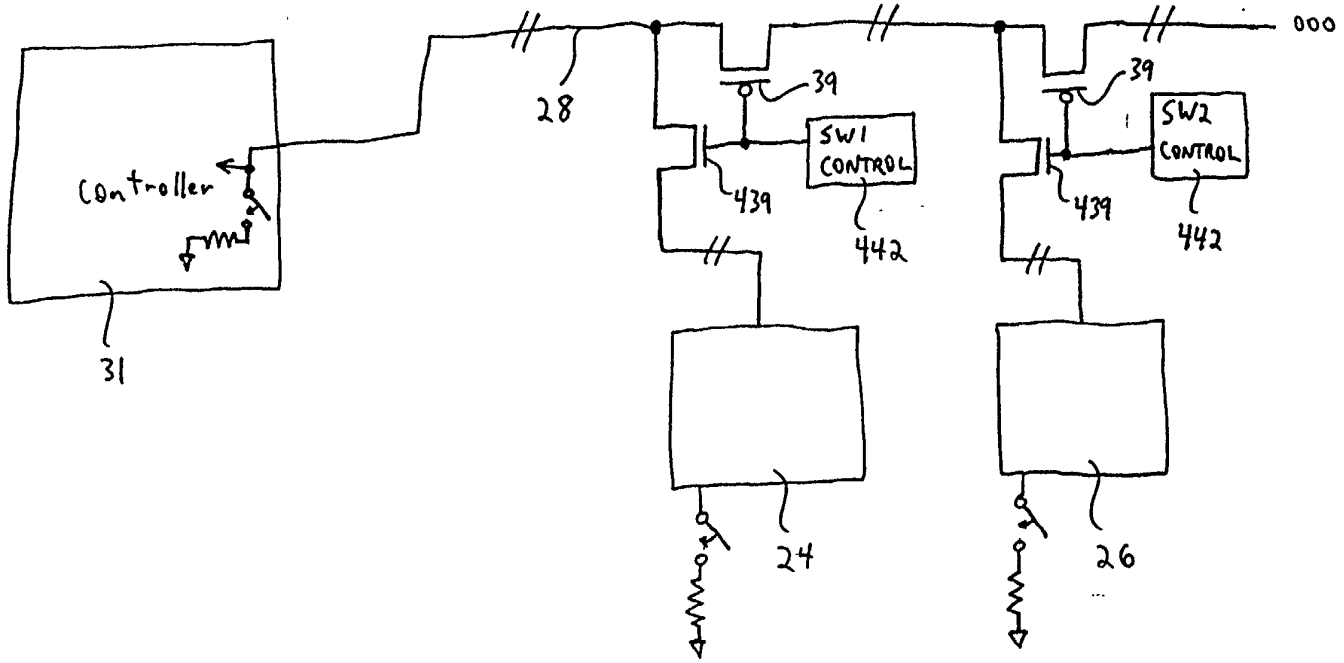
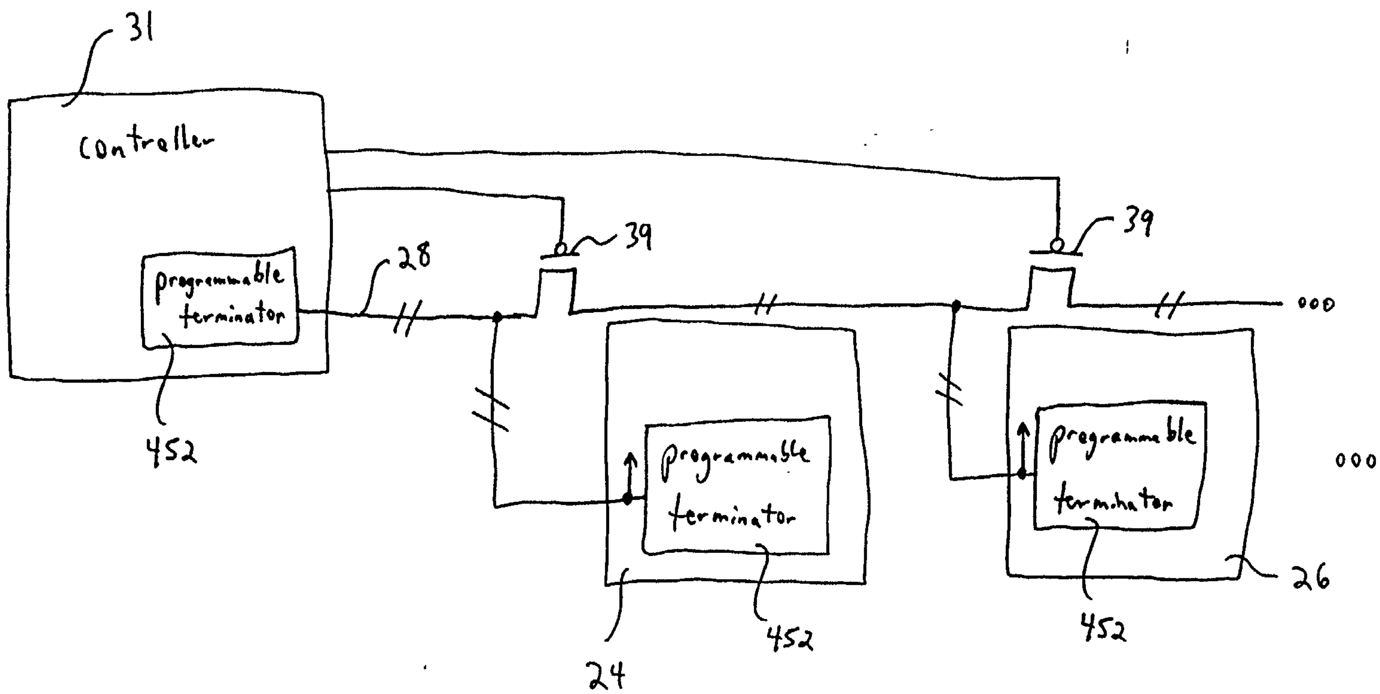


FIG. 17



31
controller
programmable terminator
452
28
39
39
programmable terminator
452
24
programmable terminator
452
26

FIG. 18